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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on September 21, 2006 has been received and entered in the case.

Election/Restrictions

2. This application contains claims 4 and 5 drawn to an invention nonelected without traverse in the reply filed on January 18, 2005 . A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
4. Claims 15 and 16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

(A) In claims 15 and 16, the specification fails to disclose the following limitation “wherein the semiconductor element is on the first conductive pattern and in direct in contact with a surface of the first conductive pattern”. Specifically, the original specification of instant invention clearly states in e.g., page 7, lines 14 – 16 “the semiconductor element 13 ... fixed to the mounting substrate 11 with **an insulating adhesive interposed therebetween**”. Thus, the phrase “direct in contact” does not have clear support in the specification of instant invention.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1 – 3 and 6 – 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi (U. S. Pat. No. 6,107,679) in view of Higashi et al. (U. S. Pat. No. 5,918,113), and further in view of Takami et al. (U. S. Pat. No. 5,126,818).

Regarding claims 1 and 6, Noguchi discloses in e.g., Fig. 7(c) a semiconductor device (the device in Fig. 7(c)), comprising:

- a mounting substrate (1; column 2, line 5) having a first main surface (the surface where the sealing resin 11 is formed) and a second main surface (the surface where the sealing resin 11 is not formed) opposite the first main surface (see Fig. 7(c)), wherein the mounting substrate (1) is a single layer (see Fig. 7(c));

- a step portion (19) in the mounting substrate (1), at a periphery of the first main surface (see Fig. 7(c)), wherein the step portion (19) extends to about the middle of the mounting substrate (1) in a thickness direction (see Fig. 7(c));
- a first conductive pattern (3; column 2, lines 8 and 9) on the first main surface of the mounting substrate (1) located inside the step portion (see e.g., Fig. 7(c));
- a second conductive pattern (2; column 2, line 7) on the second main surface of the mounting substrate (see Fig. 7(c));
- a semiconductor element (8; column 2, line 16) fixed to the first main surface of the mounting substrate and electrically connected (by wire 10) to the first conductive pattern (3); and
- sealing resin (11; column 2, lines 38 and 39) covering the first main surface of the mounting substrate and the step portion to seal the semiconductor element (see Fig. 7(c)),
- wherein a side surface of the sealing resin (11) and a side surface of the mounting substrate (1) are located on a same plane (see Fig. 7(c)).

Noguchi discloses in e.g., Fig. 7(c) does not disclose the material of the mounting substrate being resin material (claims 1 and 6). Higashi et al. teaches in e.g., Fig. 1 the material of a mounting substrate (10) being resin material (column 2, lines 7 – 9). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the resin material of Higashi et al. as the specific material to form the mounting substrate of Noguchi as taught by Higashi et al. to provide a flexibility in the mounting substrate (column 2, lines 7 – 9).

Furthermore, Noguchi and Higashi et al. do not disclose the first conductive pattern extending under the semiconductor element and to the edge of the step portion. Takami et al. teaches in e.g., Fig. 7 – Fig. 9 a conductive pattern (54; column 6, line 33) extending under a semiconductor element (55; column 6, line 42) and to the edge of a step portion (62; column 6, line 36). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to further apply the conductive pattern of Takami et al. to extend under the semiconductor element and to the edge of the step portion of Noguchi and Higashi et al. as taught by Takami et al. to prevent from being affected (column 6, lines 1 – 8).

Regarding claims 2 and 9, Noguchi discloses in e.g., Fig. 7(c) the first conductive pattern (3) comprising a bonding pad (the bonding area of 3 that is bonded to the wire 10) electrically connected to the semiconductor element (8) through a fine metallic wire (10) and a plating line (3) extending from the bonding pad to the step portion (since applicant does not specifically claim that the plating line extends toward the step portion and stops at the edge or periphery of the step portion, a reasonable interpretation of the term “extending” includes the structure taught by Noguchi). Furthermore, the term “plating” is a process designation, and would thus not carry patentable structure difference in this claim drawn to a product. See *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claims 3 and 10, Noguchi discloses in e.g., Fig. 7(c) a plurality of the bonding pads (the bonding areas of 3 that are bonded to the wire 10) being arranged so as to surround the semiconductor element (8; see Fig. 7(c)), further comprising a wiring portion (the portion of the element 3 that is formed under the chip 8) extending from each of the plurality of bonding pads under the semiconductor element (see Fig. 7(c)).

Regarding claims 7 and 12, Noguchi discloses in e.g., Fig. 7(c) the second conductive pattern comprising electrodes (2) arranged in a matrix (see Fig. 7(C)).

Regarding claims 8 and 11, Noguchi discloses in e.g., Fig. 7(c) a semiconductor device (the device in Fig. 7(c)), comprising:

- a mounting substrate (1) having a first main surface (the surface where the sealing resin 11 is formed) and a second main surface (the surface where the sealing resin 11 is not formed) opposite the first main surface (see Fig. 7(c)), wherein the mounting substrate (1) is a single layer (see Fig. 7(c));
- a step portion (19) a periphery of the first main surface of the mounting substrate (1; see Fig. 7(c)), wherein the step portion (19) extends to about the middle of the mounting substrate (1) in a thickness direction (see Fig. 7(c));
- a first conductive pattern (3) on the first main surface of the mounting substrate (1) located inside the step portion (see e.g., Fig. 7(c));
- a second conductive pattern (2) on the second main surface of the mounting substrate (see Fig. 7(c));
- a semiconductor element (8) fixed to the first main surface of the mounting substrate and electrically connected (by wire 10) to the first conductive pattern (3); and
- sealing resin (11) covering the first main surface of the mounting substrate and the step portion to seal the semiconductor element (see Fig. 7(c)),
- wherein an external side surface of the sealing resin (11) and a side surface of the mounting substrate (1) are located on a “substantially” same plane (see Fig. 7(c)).

Noguchi discloses in e.g., Fig. 7(c) does not disclose the material of the mounting substrate being resin material (claims 1 and 6). Higashi et al. teaches in e.g., Fig. 1 the material of a mounting substrate (10) being resin material (column 2, lines 7 – 9). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the resin material of Higashi et al. as the specific material to form the mounting substrate of Noguchi as taught by Higashi et al. to provide a flexibility in the mounting substrate (column 2, lines 7 – 9).

Furthermore, Noguchi and Higashi et al. do not disclose the first conductive pattern extending under the semiconductor element and to the edge of the step portion. Takami et al. teaches in e.g., Fig. 7 – Fig. 9 a conductive pattern (54; column 6, line 33) extending under a semiconductor element (55; column 6, line 42) and to the edge of a step portion (62; column 6, line 36). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to further apply the conductive pattern of Takami et al. to extend under the semiconductor element and to the edge of the step portion of Noguchi and Higashi et al. as taught by Takami et al. to prevent from being affected (column 6, lines 1 – 8).

Regarding claims 13 and 14, Noguchi, Higashi et al. and Takami et al. disclose the first conductive pattern extending laterally to the edge of the first main surface.

7. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi, Higashi et al. and Takami et al. as applied to claims 1 and 8 above, and further in view of Higuchi et al. (U. S. Pat. No. 4,835,598).

While Noguchi, Higashi et al. and Takami et al. disclose the semiconductor element being on the first conductive pattern, Noguchi, Higashi et al. and Takami et al. do not disclose the semiconductor element being in direct in contact with a surface of the first conductive pattern. Higuchi et al. teaches in e.g., Fig. 6 a semiconductor element (7; column 3, line 56) being in direct in contact with a surface of a first conductive pattern (6 or 8; column 3, lines 45 and 46). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to further apply the direct contact of Higuchi et al. between the semiconductor element and the first conductive pattern of Noguchi, Higashi et al. and Takami et al. as taught by Higuchi et al. to increase heat dissipation and to prevent the chip from being affected by any possible moisture in the substrate (column 4, lines 54 – 59).

Response to Arguments

8. Applicant's arguments with respect to claims 1 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

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the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Chris C. Chu
Examiner
Art Unit 2815



KENNETH PARKER
SUPERVISORY PATENT EXAMINER

c.c.

Wednesday, April 04, 2007